IN THE DRAWINGS:

Please enter the attached corrected drawings Figs. 1-8, in which a legend of "Prior Art" is being added in Figs. 1-4, and descriptive text is being added next to each reference number in Figs. 1-8, to replace Figs. 1-8 as originally filed. A Letter to Draftsperson is also submitted herewith.

REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated September 21, 2004. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-15 are under consideration in this application. Claims 1, 6 and 12 are being amended, as set forth above, in order to more particularly define and distinctly claim Applicants' invention.

Additional Amendments

The claims, the drawings, and the specification are being amended to correct formal errors and/or to better disclose or describe the features of the present invention as claimed. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

The drawings were objected to for the following informalities: (1) Figs. 1-4 should be labeled as "Prior Art"; (2) reference numbers 313 and 513 should be described in the specification; and (3) descriptive text should be added next to each reference number in the drawings. Claim 12 was objected to for a minor formal error.

As the drawings, the specification and the claims are being amended as suggested by the Examiner, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Allowable Subject Matter

Claims 11 and 14-15 would be allowed if they are rewritten in independent form to include all the limitations of the base and any intervening claims.

Prior Art Rejection

Claims 1-6, 10 and 12 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,608,886 to Blomgren (hereinafter "Blomgren"). Claims 7-9 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Blomgren. The prior art references of Keller (6,502,185), Hara (6,044,455), and Mahurin (6,243,805) were cited as being pertinent to the present application. These rejections have been carefully considered, but are most respectfully traversed.

The processor of the invention (e.g., Fig. 5), as recited in claim 1, comprises: an instruction fetching circuit 502 for calculating a 11-bit lower portion of an effective address 512 for a 16-bit instruction word 511 with a 12-bit displacement 204 (and a 4-bit instruction opcode 201), for replacing a value 203 of the displacement 204 in the instruction word 511 according to the 11-bit calculating result 513 (p. 11, last paragraph), and for storing the value in a storage circuit 501; and the storage circuit 501 for temporarily storing the instruction word 511, from which the stored instruction word 511 is read at an instruction execution time. The effective address 512 of said instruction word 511 in the storage circuit 501 is specified relative to a current value of a program counter address at the instruction execution time with the displacement 204. The processor utilizes the value stored in said storage 501 as a lower portion of the effective address 514 at the instruction execution time.

The instruction word 511 has the same "PC+disp" format as 112 in Fig. 2 (p. 10, last 2 lines), i.e., a 4-bit instruction opcode 201 & a 12-bit signed displacement 204, (p. 2, lines 16-22). In other words, the instruction fetching circuit 502 calculates a lower portion 512 of Fig. 5 of an effective address 512 for an instruction word 511 with displacement 204 and replaces a value of the displacement 204 in the instruction word 511 according to the calculating result 513. The displacement 204 of the instruction word 511 is replaced with the calculating result 513.

The invention, as recited in claim 6, is also directed to a processor (Fig. 5) comprising: a storage circuit 501 for temporarily storing an instruction word 511, from which the stored instruction word is read at an instruction execution time; a decoder 522 for receiving the instruction word 511 and for determining whether an effective address 512 of

said instruction word 511 is specified as a PC relative displacement value 203 therein; an adder 521 for adding of the PC relative displacement value 203 and predetermined lower bits (11 bits) of the effective address 512, and for outputting the 11-bit calculating/adding result 513 outputted from said adder as a portion of the effective address 514 if said instruction word 511 has the PC relative displacement value 203 therein; and a selector 522 for replacing the 11-bit displacement value 203 in the instruction word 501 with the 11-bit calculating/adding result 513 outputted from said adder 521, and for outputting said replaced result to said storage circuit 501 as a semiABS displacement value of the instruction word 511, if said instruction word 511 has the PC relative displacement value 203 therein.

In other words, the selector 522 replaces the displacement value 203 in the instruction word 511 with the calculating result 513.

Claim 12 recites a method which may be implemented via the embodiments recited in claim 1 or claim 6. The method for converting a first instruction word 511 with a PC relative displacement value 203 into a second instruction word 514 with a semiABS displacement value 513, comprises: calculating the semiABS displacement value 513 by adding predetermined lower bits (11 bits) of a PC address 512 and the PC relative displacement value 203; replacing the PC relative displacement value 203 in the first instruction word 511 with the calculating result 513; and storing the second instruction word 514 with the semiABS displacement value 513 in a storage circuit 501. The semiABS displacement value 513 stored in said storage circuit 501 is then immediately used as a portion of an effective address 512 at the instruction execution time.

"Program counter relative addressing" is adopted to relocate programs based on a relative distance from the current program counter (which points to the address of the currently executing instruction), instead of branching using absolute addresses. With PC relative addresses, the program can be loaded anywhere in memory and still work correctly. The location of routines, subroutines, functions, and constant data can be determined by the positive or negative distance from the current instruction. In program counter indirect with displacement operations of the invention, the new displacement value 513 is the sum of predetermined lower bits (11 bits) of the PC address and the displacement value 203 stored in the instruction. As the 1-bit value 202 is shorter than the remaining length (21-bit) of a the

processor's address space, it is sign-extended in Fig. 6 before being added with the 21-bit PC value 611 to provide the branch target address 613.

Applicants respectfully contend that Blomgren fails to teach or suggest such a "means for or step of replacing a ***displacement*** value of an instruction word *according to* or *with* the calculating result of calculating a lower portion of an effective address for the instruction word" as the invention.

Contrary to the Examiner's assertion that "this sub-address that is used as the lower part or displacement of the effective address therefore replaces the opcode displacement when written into the finder array portion of the instruction cache (4, lines 7-10 of the outstanding office action)," Blomgren merely teaches that the instruction word is loaded into the data array 24 (Fig. 6) and the sub-address 30 is generated by decoding the instruction word at the finder decoder 70 as a new code 22A (col. 10, line 50 – col. 11, line 4). Blomgren's calculating result is used to generate the new code 22A, rather than a new instruction word. The new code 22A has a format (end byte 34 + a taken bit 33 + a strong bit 32 + 2-bit type field 31 + 9 LSB of the predicted target address 30; Fig. 4A; col. 5, lines 61-65; col. 6, lines 14-37) totally different from the instruction word (a 4-bit instruction opcode 201 + a 12-bit displacement 204) of the invention.

In addition, as shown in the enclosed explanatory drawing, Blomgren processes its instruction word at the instruction decode stage 74 and the pipeline 76 (col. 11, line 55 to col. 12, line 5), while processes the new code 22A at the target predict generator 80 (col. 11, lines 46-54) separated from the ID 74 and the PL 76. Blomgren simply did NOT replace the "displacement" of the instruction word on the left side with its calculating result of the right side.

The invention only generate a mew instruction word by replacing the displacement of the old instruction word with a calculating result, but not generating any new codes deferent from the instruction words. The invention neither needs/deploys the specific Blomgren's target predict generator 80.

Blomgren fails to teach or suggest each and every feature of the present invention as recited in independent claims 1, 6 and 12. As such, the present invention as now claimed is

distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and telephone number indicated below.

Respectfully submitted,

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February 22, 2005
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